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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,002	12/09/2003	Shiva Aditham	5038-311	5864

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EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	PAPER NUMBER
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/732,002	ADITHAM, SHIVA	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Litt, U.S. Patent Number 7,051,239.

3. Regarding claim 1:

a. Regarding the limitation of "intercepting data packets," Litt discloses a system that can receive enable signals. (Lines 29-31 of Column 10).

b. Regarding the limitation of "creating error conditions responsive to the intercepting; transmitting the error conditions" Litt discloses a system that can test a process over bus lines with an OCLA used to test data on a cache over a bus. (Lines 28-38 of Column 8).

c. Regarding the limitation of "monitoring a response to the error conditions," Litt discloses a system with a monitor of the results of the test data from the OCLA to the device under test. (Lines 45-55 of Column 8).

4. Regarding claim 2, Litt discloses a system with ability to test bus routing of data from the OCLA to the cache. (Lines 40-56 of Column 11).

5. Regarding claim 3, Litt discloses a system wherein an OCLA tests memory address problems by having faulty address call. (Lines 5-24 of Column 12).

6. Regarding claim 4, Litt discloses a system wherein data is sent to an OCLA and receiving data and filtering it so it can be used in the debug mode. (Lines 36-45 of Column 8).

7. Regarding claim 5, Litt discloses a system wherein data is sent from an OCLA and receiving data, filtering it, and using it to determine operational status of the system. (Lines 45-55 of Column 8).

8. Regarding claim 6, Litt discloses a system in which the results from the monitoring are used to determine the operational function of the processor. (Lines 51-54 of Column 4).

9. Regarding claim 7:

d. Regarding the limitation of "intercepting data packets," Litt discloses a system that can receive enable signals. (Lines 29-31 of Column 10).

e. Regarding the limitation of "creating error conditions responsive to the intercepting; transmitting the error conditions" Litt discloses a system that can test a process over bus lines with an OCLA used to test data on a cache over a bus. (Lines 28-38 of Column 8).

f. Regarding the limitation of "monitoring a response to the error conditions," Litt discloses a system with a monitor of the results of the test data from the OCLA to the device under test. (Lines 45-55 of Column 8).

10. Regarding claim 8, Litt discloses a system with ability to test bus routing of data from the OCLA to the cache. (Lines 40-56 of Column 11).

11. Regarding claim 9, Litt discloses a system wherein an OCLA tests memory address problems by having faulty address call. (Lines 5-24 of Column 12).

12. Regarding claim 10, Litt discloses a system wherein data is sent to an OCLA and receiving data and filtering it so it can be used in the debug mode. (Lines 36-45 of Column 8).

13. Regarding claim 11, Litt discloses a system wherein data is sent from an OCLA and receiving data, filtering it, and using it to determine operational status of the system. (Lines 45-55 of Column 8).

14. Regarding claim 12, Litt discloses a system in which the results from the monitoring are used to determine the operational function of the processor. (Lines 51-54 of Column 4).

15. Regarding claim 13:

g. Regarding the limitation of "a processor," Litt discloses a processor core. (Lines 18-20 of Column 4).

h. Regarding the limitation of "a plurality of end points," Litt discloses a plurality of cache sets. (Lines 18-20 of Column 4).

i. Regarding the limitation of "a bridge capable of facilitating communication between the processor and the plurality of end points; a switch capable of switching between the plurality of endpoints," Litt discloses a system with an OCLA that can communicate between the CPU cores and the cache. (Lines 33-36 of Column 7 and Lines 3-6 of Column 8). The OCLA can store data in any of the cache sets under test. (Lines 12-15 of Column 5).

j. Regarding the limitation of "intercepting data packets," Litt discloses a system that can receive enable signals. (Lines 29-31 of Column 10).

k. Regarding the limitation of "creating error conditions responsive to the intercepting; transmitting the error conditions" Litt discloses a system that can test a process over bus lines with an OCLA used to test data on a cache over a bus. (Lines 28-38 of Column 8).

l. Regarding the limitation of "monitoring a response to the error conditions," Litt discloses a system with a monitor of the results of the test data from the OCLA to the device under test. (Lines 45-55 of Column 8).

16. Regarding claim 14, Litt discloses a system with ability to test bus routing of data from the OCLA to the cache. (Lines 40-56 of Column 11).

17. Regarding claim 15, Litt discloses a system wherein an OCLA tests memory address problems by having faulty address call. (Lines 5-24 of Column 12).

18. Regarding claim 16, Litt discloses a system wherein data is sent to an OCLA and receiving data and filtering it so it can be used in the debug mode. (Lines 36-45 of Column 8).

19. Regarding claim 17, Litt discloses a system wherein data is sent from an OCLA and receiving data, filtering it, and using it to determine operational status of the system. (Lines 45-55 of Column 8).

20. Regarding claim 18, Litt discloses a system in which the results from the monitoring are used to determine the operational function of the processor. (Lines 51-54 of Column 4).

21. Regarding claim 19:

m. Regarding the limitation of "intercepting data packets," Litt discloses a system that can receive enable signals. (Lines 29-31 of Column 10).

n. Regarding the limitation of "creating error conditions responsive to the intercepting; transmitting the error conditions" Litt discloses a system that can test a process over bus lines with an OCLA used to test data on a cache over a bus. (Lines 28-38 of Column 8).

o. Regarding the limitation of "monitoring a response to the error conditions," Litt discloses a system with a monitor of the results of the test data from the OCLA to the device under test. (Lines 45-55 of Column 8).

22. Regarding claim 20, Litt discloses a system with ability to test bus routing of data from the OCLA to the cache. (Lines 40-56 of Column 11).

23. Regarding claim 21, Litt discloses a system wherein an OCLA tests memory address problems by having faulty address call. (Lines 5-24 of Column 12).

24. Regarding claim 22, Litt discloses a system wherein data is sent to an OCLA and receiving data and filtering it so it can be used in the debug mode. (Lines 36-45 of Column 8).

25. Regarding claim 23, Litt discloses a system wherein data is sent from an OCLA and receiving data, filtering it, and using it to determine operational status of the system. (Lines 45-55 of Column 8).

26. Regarding claim 24, Litt discloses a system in which the results from the monitoring are used to determine the operational function of the processor. (Lines 51-54 of Column 4).

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

28. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

29. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

31. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

32. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

tmb
April 2, 2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER